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UNITED STATE PATENT AND TRADEMARK OFFICE

In re application of :
Application No. : 09/990,397
Filed : November 20,2001
For : FLASH MEMORY STRUCTURE

Examiner : LEWIS, MONICA
Art Unit : 2822

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Jiawei Huang, Reg. No. 43,330

TRANSMITTAL OF APPEAL BRIEF

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Transmitted herewith is an Appeal Brief in (8) pages, including (2) pages of Appendix, in triplicate.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

9/Appeal Brief 7-1603 Awalin

EX PARTE HSIEH et al.

Application for Patent

Filed November 20, 2001

Serial No. 09/990,397

FOR:

FLASH MEMORY STRUCTURE WITH HIGH DIELECTRIC CONSTANT LAYER

(as amended)

APPEAL BRIEF

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I. Real party in interest

The real party in interest is Macronix International Co., Ltd., the assignee of record.

II. Related appeals and interferences

There are no related appeals and/or interferences.

III. Status of the claims

A total of 12 claims were presented during prosecution of this application. Applicant appeals rejected claims 1, 2 and 4-13.

IV. Status of the amendments

A proposed after final amendment was filed by applicant on February 20, 2003, proposing amendments to the specification (Page 2, line 21), the title and Figure 1. In the Examiner's Advisory Action dated March 12, 2003 (paper #7), the Examiner indicated that the proposed amendment would be entered upon the filing of an appeal.

V. Summary of the invention

In light of the trend in portable electronic products, the demand for flash memory has noticeably increased. The memory card of a digital camera, the memory of a personal electronic notebook, personal MP3 walkman, electronic answering machine and a programmable IC are all parts of the market for flash memory applications. The flash memory using an oxide-nitride-oxide (ONO) stacked layer as a dielectric layer between the floating gate and the control gate, can be written in four states within a single memory cell, thus serving as a 1 cell 2 bit flash memory.

The present invention provides a flash memory structure using a high electric constant dielectric layer as a material for the dielectric stacked layer, so that the dielectric constant and

capacitance of the dielectric stacked layer are increased. Accordingly, the gate coupling ratio is increased and voltage required in operating the flash memory is reduced, thus decreasing energy consumption.

The flash memory structure of the present invention includes a tunneling oxide layer, a floating gate, a dielectric stacked layer, a control gate and a source/drain region. The dielectric stacked layer is formed by successively stacking a first oxide layer, a dielectric layer with a high dielectric constant material and a second oxide layer, and is located between the floating gate and the control gate. High dielectric constant dielectric used in the present invention refers to a dielectric material that has a dielectric constant greater than the dielectric constant of Si_3N_4/SiO_2 (NO). The second oxide layer between the high dielectric constant dielectric layer and the control gate, or even the first oxide layer, can be omitted, if the band gap of the utilized high dielectric constant dielectric layer is about as wide or wider than the silicon oxide band gap.

VI. Issues

Were claims 1, 2 and 4-13 properly rejected under 35 U.S.C. 103(a) as being obvious over Park in view of Bui?

VII. Grouping of the claims

Applicant proposes all claims stand or fall together.

VIII. Arguments

A. The related law

A prima facie case of obviousness requires that the reference teachings "appear to have suggested the claimed subject matter." *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143, 147 (CCPA 1976). To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

When more than one reference or source of prior art is required in establishing the obviousness rejection, "it is necessary to ascertain whether the prior art teachings would appear to be sufficient to one of ordinary skill in the art to suggest making the claimed substitution or other modification." *In re Lalu*, 747 F.2d 703, 223 USPQ 1257, 1258 (Fed. Cir. 1984). There must be some motivation to combine the references; this motivation must come from "the nature of the problem to be solved, the teachings of the prior art, [or] the knowledge of persons of ordinary skill in the art." *In re Rouffet*, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998).

Finally, if an independent claim is nonobvious under 35 U.S.C.§103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d, 1596 (Fed. Cir. 1988).

B. *Claims 1, 2 and 4-13 were improperly rejected under 35 U.S.C. 103(a) as being unpatentable over Park in view of Bui.*

1. The rejection

All of the claims on appeal have been rejected under 35 USC §103(a) over Park (U.S. Patent No. 6,100,559; hereinafter "Park") in view of Bui (U.S. Patent No. 6,163,049; hereinafter "Bui"). In making the rejection, the Examiner has construed Park to disclose the memory structure except a dielectric constant of the high dielectric constant layer being greater than 8. The Examiner cites Bui to teach a dielectric layer composed of aluminum oxide, which has a dielectric constant greater than 8.

2. The prior art

Park discloses a memory cell 8, including a doped substrate 12, a source/drain 13a, 13b, a tunnel oxide layer 15 and an interpoly dielectric 24 separating a floating gate 16 from a control gate 26. Floating gates are separated by field oxides (FOX) 14a-b. Park states that the interpoly dielectric 24 typically includes a plurality of films, such as, a bottom film of silicon dioxide, a middle film of silicon nitride and a top film of silicon dioxide. This type of interpoly dielectric is commonly referred to as an oxide-nitride-oxide (ONO) layer (Col. 2,

lines 20-25). Interpoly dielectric layer 24 has been conformally deposited over the exposed portions of floating gates 16a-c and field oxides 14a-b.

Bui teaches a composite interpoly dielectric layer of a nonvolatile memory device. The composite ONO dielectric film 600 is between a floating gate 500 and a control gate 700. The composite **ONO** film stack 600 includes a LPCVD silicon dioxide layer 601, a silicon nitride layer 602 and a second oxide layer 603 comprising a material with a dielectric constant greater than that of silicon dioxide, e.g., greater than about 10, such as aluminum oxide, titanium oxide or tantalum oxide. Alternatively, the composite **ONO** film stack 660 includes a first oxide layer 661, a silicon nitride layer 662 and a second oxide layer 663, while both oxide layers 661/663 comprising a material with a dielectric constant greater than that of silicon dioxide, e.g., greater than about 10, such as aluminum oxide, titanium oxide or tantalum oxide. Bui teaches enabling deposition of one or both oxide layers of the composite ONO film to a thickness greater than the design rule by utilization of a material with a dielectric constant greater than 10, thus allowing greater flexibility in oxide deposition.

3. The prior art differentiated

What significantly distinguishes the structure of this invention is the high dielectric constant dielectric layer having a dielectric constant larger than 8, which is between the oxide layers of the interpoly dielectric stacked layer. In the old style, and in both Park and Bui, the interpoly dielectric layer is an ONO layer. The purpose of the present invention is to reduce the voltage value required in operating the flash memory and minimize energy consumption.

Park merely teaches forming the ONO layer as the interpoly dielectric layer between the control gate and the floating gate. Likewise, Bui discloses an oxide/silicon nitride/oxide layer, with the **silicon nitride layer sandwiched between two oxide layers** as a composite film stack. Neither Park nor Bui teach or suggest the high dielectric constant dielectric layer having a dielectric constant greater than 8 between the oxide layers.

An equally important and related difference between this invention and the cited prior art is that the high dielectric constant dielectric layer be possible between the control gate and the floating gate without oxide layers in-between. The oxide layers are used to enhance adhering ability between the high dielectric constant dielectric layer, the floating

gate and the control gate and minimize the occurrence of defects. The oxide layers on or below the high dielectric constant dielectric layer can be omitted, if the band gap of the high dielectric constant dielectric layer is about as wide or wider than the silicon oxide band gap. Park does not teach or suggest the band gap value or the criterion for the exclusion of the oxide layer. Contrary to this invention, one of Bui's important features is to increase the thickness of the oxide layers in the composite ONO film, so that the oxide layers in the composite ONO film of Bui's has to be included and can not be omitted under any circumstances.

4. No motivation to combine Park and Bui

The Office Action combines Park with Bui to modify the device of Park to include the aluminum oxide of Bui in order to maintain the capacitance of the ONO film. But that is contrary to the teachings of these references, because Park discloses the silicon oxide/silicon nitride/silicon oxide (ONO) layer between the floating gate and the control gate and Bui suggests the silicon nitride layer sandwiched between two high dielectric oxide layers (also ONO). Obviously, if combining Park and Bui, one of ordinary skill in the art will form a stacked ONO layer consisting of aluminum oxide/silicon nitride/aluminum oxide, since Bui's high dielectric oxide layers will replace two silicon oxide layers in the ONO layer of Park's. Therefore, the combination of Park and Bui can not arrive at this invention.

In the present invention, the use of the high dielectric constant dielectric layer increases the capacitance of the dielectric stacked layer and increases the gate coupling ratio, thus reducing the applied voltage to the control gate. However, Bui teaches forming thicker oxide layers of the composite ONO film by using a material with a dielectric constant greater than 10, so that the capacitance of the composite ONO film is maintained and the operating voltage of the device does not change. Therefore, Bui in fact teaches away from this invention because Bui teaches maintaining the capacitance and not changing the operating voltage.

IX. Conclusion

As noted, none of the cited art, either alone or in combination, can be said to render obvious the appealed claims. Neither Park nor Bui teaches the dielectric stacked layer having

the high dielectric constant dielectric layer with the dielectric constant greater than 8 between the oxide layers. No combination of Park or Bui can provide the dielectric stacked layer for the reduction of applied voltage and minimization of energy consumption as taught in the present invention.

Accordingly, Applicant believes that the rejections under 35 U.S.C.§103 are in error, and respectfully requests the Board of Patent Appeals and Interferences to reverse the Examiner's rejections of the claims on appeal.

Respectfully submitted,
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Date: 6/27/2003

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APPENDIX A - CLAIMS ON APPEAL

WHAT IS CLAIMED IS:

1. (Once Amended) A flash memory structure, comprising:

a tunneling oxide layer located upon a substrate;

a floating gate located upon the tunneling oxide layer;

a first oxide layer located upon the floating gate;

a high dielectric constant dielectric layer located upon the first oxide layer, wherein a dielectric constant of the high dielectric constant dielectric layer is greater than 8;

a second oxide layer, located upon the high dielectric constant dielectric layer, wherein, together with the first oxide layer and the high dielectric constant dielectric layer, a dielectric stacked layer is formed;

a control gate formed on the second oxide layer of the dielectric stacked layer; and

a source/drain region located in the substrate on the two sides of the floating gate.

2. The flash memory structure as defined in claim 1, wherein a band gap value of the high dielectric constant dielectric layer is less than a band gap value of silicon oxide.

3. Cancelled.

4. The flash memory structure as defined in claim 1, wherein the high dielectric constant dielectric layer is a single layer including one material selected from the group consisting of Al_2O_3, Y_2O_3, $ZrSi_xO_y$, $HfSi_xO_y$, La_2O_3, ZrO_2, HfO_2, Ta_2O_5, Pr_2O_3 and TiO_2.

5. The flash memory structure as defined in claim 1, wherein the high dielectric constant dielectric layer is a layer including a mixed material any one selected from the group consisting of Al_2O_3, Y_2O_3, $ZrSi_xO_y$, $HfSi_xO_y$, La_2O_3, ZrO_2, HfO_2, Ta_2O_5, Pr_2O_3 and TiO_2.

6. The flash memory structure as defined in claim 1, wherein the material of the high dielectric constant dielectric layer is stacked layer, each layer of the stacked layer including one selected from the group consisting of Al_2O_3, Y_2O_3, $ZrSi_xO_y$, $HfSi_xO_y$, La_2O_3, ZrO_2, HfO_2, Ta_2O_5, Pr_2O_3 and TiO_2.

7. (Once Amended) A flash memory structure, comprising:

a tunneling oxide layer located upon a substrate;

a floating gate located upon the tunneling oxide layer;

a first oxide layer located upon the floating gate;

a high dielectric constant dielectric layer having a dielectric constant greater than 8 located upon the first oxide layer, wherein, together with the oxide layer, a dielectric stacked layer is formed;

a control gate formed on the high dielectric constant dielectric layer of the dielectric stacked layer; and

a source/drain region located within the substrate on the two sides of the floating gate.

8. The flash memory structure as defined in claim 7, wherein a band gap value of the high dielectric constant dielectric layer is greater than a band gap of silicon oxide.

9. The flash memory structure as defined in claim 7, wherein a band gap value of the high dielectric constant dielectric layer is equivalent to a band gap of silicon oxide.

10. The flash memory structure as defined in claim 7, wherein the high dielectric constant dielectric layer is a single layer including one material selected from the group consisting of Al_2O_3, Y_2O_3, $ZrSi_xO_y$, $HfSi_xO_y$, La_2O_3, ZrO_2, HfO_2, Ta_2O_5, Pr_2O_3 and TiO_2.

11. The flash memory structure as defined in claim 7, wherein the high dielectric constant dielectric layer includes a mixed material selected from any one of the group consisting of Al_2O_3, Y_2O_3, $ZrSi_xO_y$, $HfSi_xO_y$, La_2O_3, ZrO_2, HfO_2, Ta_2O_5, Pr_2O_3 and TiO_2.

12. The flash memory structure as defined in claim 7, wherein the high dielectric constant dielectric layer is a stacked layer, each layer of the stacked layer including one selected from the group consisting of Al_2O_3, Y_2O_3, $ZrSi_xO_y$, $HfSi_xO_y$, La_2O_3, ZrO_2, HfO_2, Ta_2O_5, Pr_2O_3 and TiO_2.

13. A flash memory structure, comprising:

a tunneling oxide layer located upon a substrate;

a floating gate located upon the tunneling oxide layer;

an Al_2O_3 layer located upon the floating gate;

a control gate located upon the Al_2O_3 layer; and

a source/drain region located within the substrate on the two sides of the floating gate.